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10/708,354	02/26/2004	Yang-En Wu	ADTP0092USA	2353

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EXAMINER	
NGUYEN, THANH NHAN P	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,354	WU, YANG-EN	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P. Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

Paragraphs 0021-0026, 0029, and 0032 presently read as "Fig."; please insert the number figure, such as "Fig. 5", "Fig. 6", etc. properly.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamakita et al U.S. Patent Application Publication No. 2002/0154262 in view of Liu et al U.S. Patent Application Publication No. 2001/0050745.

Referring to claims 1, Yamakita et al discloses an in-plane switching mode liquid crystal display (IPS-LCD) comprising:

- a lower substrate (1A);
- a plurality of parallel scan lines (6) and a plurality of data lines (5) with equal distances positioned on the lower substrate, wherein the scan lines and the data lines are arranged in a crossing manner to form a pixel

matrix, any two of the adjoining scan lines and any two of the adjoining data lines being crossed to define a pixel;

- a plurality of first electrodes (3) formed in each of the pixels, wherein each of the first electrodes contains a plurality of first electrode offshoots (3a, 3b, 3c), the first electrode offshoots being arranged parallel with each other;
- an insulation layer (12) covering the scan lines and the first electrodes;
- a plurality of second electrodes (4) formed in each of the pixels;
- an upper substrate (1B) formed in parallel with and opposite to the lower substrate;
- and a plurality of liquid crystal molecules (2) filled between the upper substrate and the lower substrate.

[see figs. 12(a)-12(c)]

Yamakita et al lacks disclosure of each of the second electrodes covers at least one of the first electrode offshoots in each of the pixels; and wherein an overlapping portion of each of the first electrode offshoots and each of the second electrode serves as a storage capacitor of each of the pixels.

Liu et al discloses each of the second electrodes (145a, 146a) covers at least one of the first electrode offshoots (124a, 125a) in each of the pixels; and wherein an overlapping portion of each of the first electrode offshoots and each of the second electrode serves as a storage capacitor of each of the pixels, [see fig. 8], for the benefit of increasing the capacitance of the storage capacitor, and increasing the aperture ratio

of the pixel device, [see par. 0010]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have each of the second electrodes covers at least one of the first electrode offshoots in each of the pixels for the benefit of increasing the capacitance of the storage capacitor, and increasing the aperture ratio of the pixel device.

Referring to claim 4, Yamakita et al lacks disclosure of each of the second electrodes contains a plurality of second electrode offshoots, each of the second electrode offshoots being arranged parallel with the first electrode offshoots and covering one of the first electrode offshoots in each of the pixels.

Liu et al discloses each of the second electrodes contains a plurality of second electrode offshoots (145a, 146a), each of the second electrode offshoots (145a) being arranged parallel with the first electrode offshoots (124a, 125a) and covering one of the first electrode offshoots (124a) in each of the pixels, [see fig. 8], for the same benefit as discussed in claim 1.

Referring to claim 2, Yamakita et al discloses the first electrode offshoots are parallel with the data lines in each of the pixels, [see fig. 12b].

Referring to claim 3, Yamakita et al discloses the second electrodes partially cover the scan lines, an overlapping portion of each of the second electrodes and each of the scan lines serving as the storage capacitor of each of the pixels, [see fig. 12b].

Referring to claim 5, the language regarding the use as a polarizer is an intended use limitation, and therefore does not patentably distinguish the invention. Besides, Yamakita et al discloses a first polarizer (102) and a second polarizer (102) positioned on an upper surface of the upper substrate and a bottom surface of the lower substrate respectively, [see fig. 23a].

Referring to claim 6, Yamakita et al discloses a first alignment film (9B) and a second alignment film (9A) on a bottom surface of the upper substrate and an upper surface of the lower substrate respectively, [see fig. 12b].

Referring to claim 7, Yamakita et al discloses each of the pixels further comprises a thin film transistor (7), the TFT serving as a switching device of the pixel, [see fig. 12b].

Referring to claims 8-9, Yamakita et al discloses each of the first electrodes (3) is used as a common electrode in each of the pixels; and each of the second electrodes (4) is used as a pixel electrode in each of the pixels, [see par. 0099].

Referring to claims 10 and 11, Yamakita et al discloses each of the first electrodes and each of the second electrodes are disposed in a single-layer structure or a multi-layer structure, and comprise indium tin oxide (ITO), or other conductive materials, [see par. 0102].

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamakita et al in view of Liu et al as discussed above, and further in view of Aoyama et al U.S. Patent Application Publication No. 2003/0043327.

Referring to claim 12, Yamakita et al lacks disclosure of the data lines, the first electrode offshoots, and the second electrodes are bended lines.

However, it was well known that the in-plane switch (IPS) display mode having a structure in which electrodes and wiring groups on the substrate are bent in zigzag shapes is called multi-domain IPS, and it is used to overcome the color tone varies with the visual angle problem in conventional IPS display mode, [see fig. 3; pars. 0005-0009], as evidenced by Aoyama et al. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the data lines, the first electrode offshoots, and the second electrodes are bended lines for the benefit of overcoming the color tone varies with the visual angle problem in conventional IPS display mode.

Claims 13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamakita et al U.S. Patent Application Publication No. 2002/0154262 in view of Lee et al U.S. Patent Application Publication No. 2004/0109120.

Referring to claim 13, Yamakita et al discloses an in-plane switching mode liquid crystal display (IPS-LCD) comprising:

- a lower substrate (1A);
- a plurality of parallel scan lines (6) and a plurality of data lines (5) with equal distances positioned on the lower substrate, wherein the scan lines and the data lines are arranged in a crossing manner to form a pixel

matrix, any two of the adjoining scan lines and any two of the adjoining data lines being crossed to define a pixel;

- a plurality of first electrodes (3) formed in each of the pixels, wherein each of the first electrodes contains a plurality of first electrode offshoots (3a, 3b, 3c), the first electrode offshoots being arranged parallel with each other;
- an insulation layer (12) covering the scan lines and the first electrodes;
- a plurality of second electrodes (4) formed in each of the pixels;
- an upper substrate (1B) formed in parallel with and opposite to the lower substrate;
- and a plurality of liquid crystal molecules (2) filled between the upper substrate and the lower substrate.

[see figs. 12(a)-12(c)]

Yamakita et al lacks disclosure a plurality of capacitor electrodes arranged parallel with the first electrode offshoots in the pixels, each of the pixels comprising at least one of the capacitor electrodes; each of the second electrodes covering at least one of the capacitor electrodes formed in each of the pixels; wherein an overlapping portion of each of the second electrodes and each of the capacitor electrodes serves as a storage capacitor of each of the pixels.

Lee et al discloses a plurality of capacitor electrodes (56) arranged parallel with the first electrode offshoots (54) in the pixels, each of the pixels comprising at least one of the capacitor electrodes; each of the second electrodes (64) covering at least one of

the capacitor electrodes formed in each of the pixels; wherein an overlapping portion of each of the second electrodes and each of the capacitor electrodes serves as a storage capacitor of each of the pixels, [see fig. 7B], for the benefit of solving the demerits of shot mura and flicker in in-plane switching liquid crystal display device, [see par. 0012]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a plurality of capacitor electrodes arranged parallel with the first electrode offshoots in the pixels; and each of the second electrodes covering at least one of the capacitor electrodes formed in each of the pixels for the benefit of solving the demerits of shot mura and flicker in in-plane switching liquid crystal display device.

Referring to claim 16, Yamakita et al lacks disclosure each of the second electrodes comprises a plurality of second electrode offshoots, each of the second electrode offshoots being arranged parallel with the first electrode offshoots and covering one of the capacitor electrodes formed in each of the pixels.

Lee et al discloses each of the second electrodes comprises a plurality of second electrode offshoots, each of the second electrode offshoots (64) being arranged parallel with the first electrode offshoots (54) and covering one of the capacitor electrodes (56) formed in each of the pixels, [see fig. 7B], for the same benefit as discussed in claim 13.

Referring to claim 14, Yamakita et al discloses the first electrode offshoots are parallel with the data lines in each of the pixels, [see fig. 12b].

Referring to claim 15, Yamakita et al discloses the second electrodes partially cover the scan lines, an overlapping portion of each of the second electrodes and each of the scan lines serving as the storage capacitor of each of the pixels, [see fig. 12b].

Referring to claim 17, the language regarding the use as a polarizer is an intended use limitation, and therefore does not patentably distinguish the invention. Besides, Yamakita et al discloses a first polarizer (102) and a second polarizer (102) positioned on an upper surface of the upper substrate and a bottom surface of the lower substrate respectively, [see fig. 23a].

Referring to claim 18, Yamakita et al discloses a first alignment film (9B) and a second alignment film (9A) on a bottom surface of the upper substrate and an upper surface of the lower substrate respectively, [see fig. 12b].

Referring to claim 19, Yamakita et al discloses each of the pixels further comprises a thin film transistor (7), the TFT serving as a switching device of the pixel, [see fig. 12b].

Referring to claims 20-21, Yamakita et al discloses each of the first electrodes (3) is used as a common electrode in each of the pixels; and each of the second electrodes (4) is used as a pixel electrode in each of the pixels, [see par. 0099].

Referring to claims 22-23, Yamakita et al discloses each of the first electrodes and each of the second electrodes are disposed in a single-layer structure or a multi-layer structure, and comprise indium tin oxide (ITO), or other conductive materials, [see par. 0102].

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamakita et al in view of Lee et al as discussed above, and further in view of Aoyama et al U.S. Patent Application Publication No. 2003/0043327.

Referring to claim 24, Yamakita et al lacks disclosure of the data lines, the first electrode offshoots, the second electrodes, and the capacitor electrodes are bended lines.

However, it was well known that the in-plane switch (IPS) display mode having a structure in which electrodes and wiring groups on the substrate are bent in zigzag shapes is called multi-domain IPS, and it is used to overcome the color tone varies with the visual angle problem in conventional IPS display mode, [see fig. 3; pars. 0005-0009], as evidenced by Aoyama et al. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the data lines, the first electrode offshoots, and the second electrodes are bended lines for the benefit of overcoming the color tone varies with the visual angle problem in conventional IPS display mode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamakita et al U.S. Patent Application Publication No. 2002/0154262 discloses an in-plane switching LCD device having the pixel electrodes overlapping the scanning lines; and the common electrodes, and pixel electrodes are bended lines.

Liu et al U.S. Patent Application Publication No. 2001/0050745 discloses the pixel electrodes overlapping at least one the common electrode offshoots.

Lee et al U.S. Patent Application Publication No. 2004/0109120 discloses the pixel electrodes overlapping at least one of the capacitor electrodes.

Aoyama et al U.S. Patent Application Publication No. 2003/0043327 discloses the multi-domain in-plane switching display mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 28, 2005
TN

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